Code No: **R32045** **R10** **Set No. 1**

III B.Tech II Semester Supplementary Examinations, Dec - 2015

VLSI DESIGN

(Common to ECE and EIE)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1	a)	With neat sketches explain oxidation process in IC fabrication.	[8]
	b)	List out Differences between CMOS and bipolar technologies	[7]
2	a)	Explain Latch-up in CMOS circuits	[7]
	b)	Determine Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter.	[8]
3	a)	Explain the basic operation of CMOS logic gate.	[5]
	b)	What is stick diagram? Explain about different symbols used for components in stick diagram	[10]
4	a)	Explain about the concepts of Sheet Resistance.	[7]
	b)	Define and explain the standard units of capacitance.	[8]
5	a)	Write the scaling factors for different types of device parameters.	[8]
	b)	Is scaling is a required parameter? Explain with reason.	[7]
6	a)	Explain about configurable FPGA based I/O blocks.	[5]
	b)	What is CPLD? Draw its basic structure and give its applications.	[10]
7		Design the process of digital system and VLSI circuit.	[15]
8	a)	What is the format of major netlist for design representation?	[8]
	b)	What is shift register? Write VHDL code for shift register.	[7]

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